A 4.8-mW 10-Mb/s Wideband Signaling Receiver Analog Front-End for Human Body Communications

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***Abstract*—This paper presents an energy-efficient receiver AFE to recover binary data from the feeble wideband pulse signals through the human body as a data transmission medium. The receiver AFE exploiting wideband symmetric triggering technique delivers data at 10-Mb/s rate with the input sensitivity of -27-dBm and the operational bandwidth of about 200-MHz. The on-chip symmetric bias circuit provides 50-Ω input impedance for high-speed symmetric operation leading to low power consumption. The proposed operational amplifier is based on the low-voltage fully complementary folded cascode topology. It exhibits 60-dB DC gain and 684-MHz GBW with 1.5-mA dissipation. The 0.18-μm CMOS receiver AFE occupies 0.04-mm^2 and consumes only 4.8-mW from a 1-V supply.**

I. INTRODUCTION

Recently, the on-body networks have been widely studied for heath monitoring and wearable computing applications around the human body [1]-[2]. In their applications, the portable or wearable electronic devices (e.g., wrist-type computer, video eyeglass, and head-mounted display), which have been worn around the human body and powered by a very small battery, require a low power receiver employing energy-efficient communication schemes. Moreover, the high data rate operation needs for receiving multimedia data such as audio or video using on-body networks.

There are two candidates using a radio frequency (RF)-based communication for on-body networks: Bluetooth and ultra wideband (UWB). Bluetooth technology is not available for the transmission of multimedia data due to huge power consumption and insufficient data rate of 1-Mb/s. Even the Zero-G receiver [3] to achieve significant power savings over the Bluetooth radios consumes still too high power. Alternatively, the UWB receivers have been widely developed to achieve higher data rate operation, but must operate at vast bandwidth inherently leading to increase of power dissipation. For example, according to [4], an UWB receiver based on impulse radio was reported with power consumption of about 30-mW at 3-to-5GHz bandwidth for wearable and wireless body area networks. In addition, it faces increasing cost for additional RF process, severe interference problem at very short range around human body, and FCC regulation.

To overcome the problems of such RF-based receivers for on-body networks, the novel communication method using a human body as a data transmission medium, called human body communication (HBC), was proposed in [2], [5]-[6]. The HBC receiver firstly introduced in [5] integrates the tiny current with a single carrier frequency of 330-kHz and has limited data rate of 2.4-kb/s. The recently developed HBC receiver [6] requires a special electrooptic sensor to achieve 10-Mb/s data rate, and also it consumes too high power to apply for human body applications.

In order to achieve lower power consumption with high data rate operation, the novel HBC scheme, wideband signaling (WBS), was proposed in [2]. Fig. 1 shows the block diagram of the HBC based on WBS. Following the previous study of [2], this paper presents a 10-Mb/s WBS receiver analog front-end (AFE) exploiting wideband symmetric triggering (WST) technique that efficiently recovers binary data from the feeble wideband pulse signals. The AFE incorporates with a low-power wideband op amp based on the low-voltage fully complementary folded cascode topology. Realized in a 0.18-μm standard CMOS technology, the AFE occupies 0.04-mm^2 and exhibits power consumption less than 5-mW from a 1-V supply. Accordingly, the proposed AFE is suitable for the application to energy-efficient transmission of multimedia data around the human body.

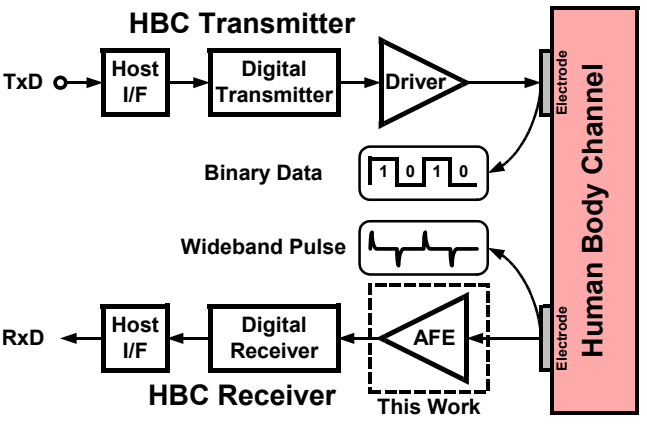

Figure 1. Human body communication based on wideband signaling.

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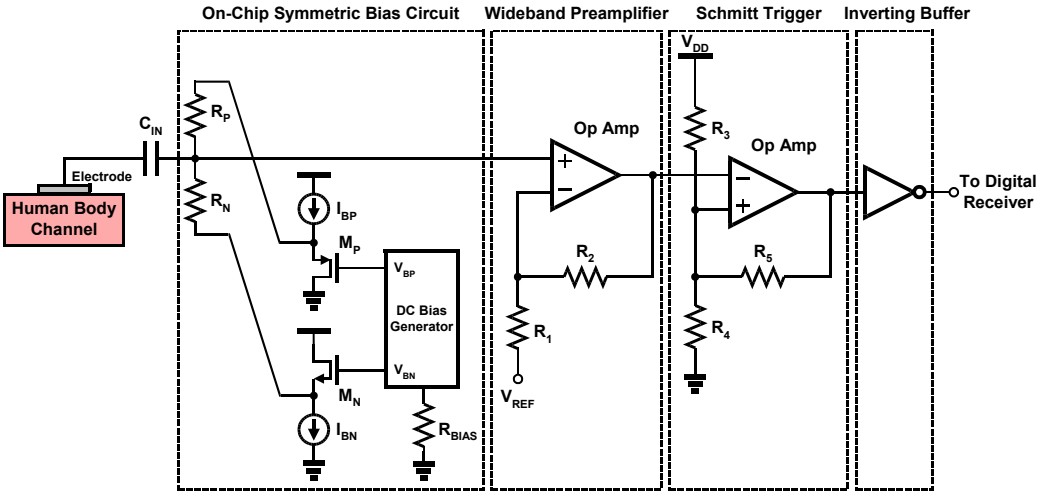

Figure 2. Wideband signaling receiver analog front-end.

II. WBS RECEIVER AFE

The characteristics of the human body channel were investigated with the WBS scheme as described in [2]. When the binary data directly applies to the human body with a single electrode, the output of the channel exhibits narrow small pulse signals with no DC offset. These characteristics have some analogy to the AC-coupled chip-to-chip interconnect using 50-Ω transmission lines on a FR-4 PC board shown in [7]. The pulse receiver used in the AC-coupled interconnect achieves high data rate of several Gb/s. However, it should be based on differential structure with poor receiver sensitivity more than 100-mV from a 1.8-V supply. However, for the HBC, the supply voltage is limited to 1-V for longer battery life. According to the investigation in [2], the input sensitivity of a receiver AFE needs to be less than 10-mV, which corresponding to -27-dBm for the 50-Ω input impedance. In order to recover binary data from the narrow small pulse signals over the human body channel, the WBS receiver AFE in this work exploits WST technique. Thus, the proposed AFE achieves not only high data rate operation and also lower input sensitivity with a 1-V supply. Fig. 2 shows the block diagram of the proposed receiver AFE consisting of four blocks: an on-chip symmetric bias circuit, a wideband preamplifier, a schmitt trigger, and an inverting buffer. The AC coupling capacitor is connected to the input of the AFE. This capacitor eliminates the conductive current path to the body and provides DC biasing for the input of the preamplifier regardless of the body's potential. The capacitance of C_{IN} with the input impedance of the on-chip bias circuit determines low 3-dB frequency of the AFE. The on-chip bias circuit is designed as a complementary configuration to acquire symmetric impedance of 50-Ω and DC biasing with no external bias circuit. Hence, the on-chip symmetric bias circuit comprises pull-up resistor R_P, pull-down resistor R_N, a pair of complementary source followers (I_{BP}-M_P, I_{BN}-M_N), and a DC bias generator controlled by a resistor R_{BIAS}. The input impedance of the AFE R_{IN} can be expressed as:

$$R_{IN} = \left(\frac{1}{g_{mP}} + R_P\right) // \left(\frac{1}{g_{mN}} + R_N\right) \approx \frac{1/g_m + R}{2}, \qquad (1)$$

where g_{mP} and g_{mN} are the transconductance of M_P and M_N, respectively, R_P=R_N=R and g_{mP}=g_{mN}=g_m for symmetric design. From (1), the effect of $1/g_m$ and R variations can be alleviated by half. Addition of the resistor R_P and R_N achieves not only high rejection to power supply noise that may corrupt the received signal, but also reduction of the variation of $1/g_{mP}$ and $1/g_{mN}$ due to large swing of the received signal. According to the simulations, the on-chip symmetric bias circuit dissipates 1.8-mA, which is 36% of the power consumed by using only the pull-up and pull-down resistors without M_p and M_N. The wideband preamplifier is designed as a non-inverting amplifier where the op amp incorporates the low power wideband configuration. The high 3-dB frequency of the AFE is constrained by the 3-dB bandwidth of the preamplifier. Since the power spectrum of the received signal remains below 200-MHz, the preamplifier requires the 3-dB bandwidth of 200-MHz. the schmitt trigger consists of three resistors (R_3-R_5) and the same op amp as that of the preamplifier and produces positive and negative triggering thresholds (V_{TH} and V_{TL}), which can be controlled by varying the resistance of R_5. With R_4=R_3, the sum of two triggering thresholds is equal to the supply voltage. Hence, the minimum input sensitivity of the receiver AFE $(V_{RXSEN})_{\min}$ is given by

$$(V_{RXSEN})_{\min} = \frac{V_{TH} - V_{DD}/2}{A_V} = \frac{R_3}{2(R_3 + 2R_5)} \frac{V_{DD}}{A_V}, \qquad (2)$$

where V_{DD} is the supply voltage of the AFE and A_V is the voltage gain of the preamplifier, given as $1+R_2/R_1$. As the supply voltage decreases and the voltage gain of the preamplifier increases, the input sensitivity of the AFE can be minimized.

Fig. 3 illustrates the timing diagrams for the operation of the receiver AFE exploiting WST technique. As explained before, the channel output for the transmitted binary data is

the narrow small pulse signal that comprises positive and negative pulses. The received pulse signal corrupted by the channel is sufficiently amplified for wide bandwidth, and subsequently, the signal is triggered to positive and negative states by using two symmetric thresholds, V_{TH} and V_{TL}, where the symmetric operation provides the duty cycle of 50%. Consequently, the binary data can be recovered by inverting the triggered signal.

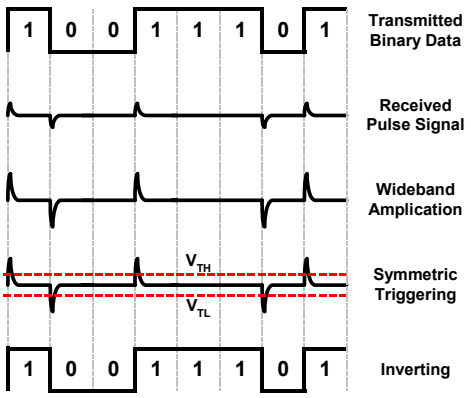

Figure 3. Timing diagrams of the receiver AFE operation exploiting WST.

III. Low Power Widebnad Op Amp

The wide bandwidth operation in the AFE leads to increase of power consumption. Decreasing supply voltage is very attractive to reduce the power consumption [8]. But, the supply voltage, 1-V in this work, is lower than the sum of the threshold voltage of the NMOS and PMOS. This makes it difficult to design a low-voltage and wideband op amp. To alleviate this difficulty, the low-voltage fully complementary folded cascode topology is proposed in this work. Fig. 4 shows the proposed topology, consisting of an input stage with the source follower pairs, a gain stage employing fully complementary input pairs with low-voltage folded cascode loads, and a cross-coupled class-AB output stage. All configurations of the op amp are based on complementary structure for symmetric operation. The source follower input pairs need to obtain the sufficient overdrive voltage and to minimize the area overhead at the gain stage. The gain stage employs the fully complementary differential pair and the low-voltage folded cascode configurations. Particularly, the complementary low-voltage loads with each output can further reduce the number of the stacked transistors than the configuration with single output load. A class-AB output stage has been widely chosen to minimize quiescent power consumption leading to a fast operation with high slew rate. The cross-coupled type of the class-AB is adopted in accordance with the fully complementary gain stage. Fig. 5 shows the transistor-level implementation of the proposed low power wideband op amp. According to the simulations, it exhibits 60-dB DC gain and the gain bandwidth product of 684-MHz while dissipating only 1.5-mW with a 1-V supply. With the help of the cross-coupled class-AB, its slew rate is 880-V/μs. Its performance is summarized in table I.

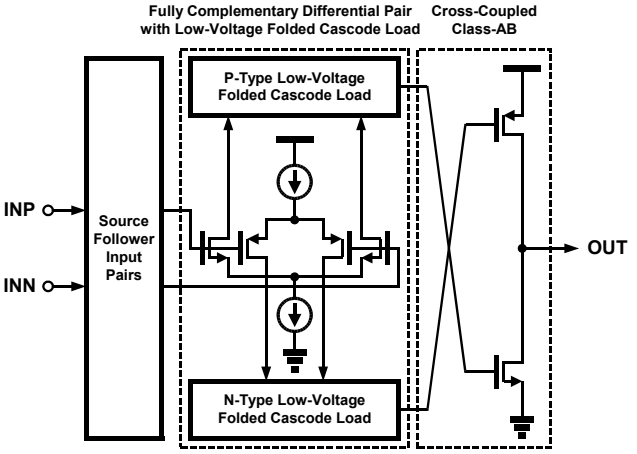

Figure 4. Low-voltage fully complementary folded cascode topology.

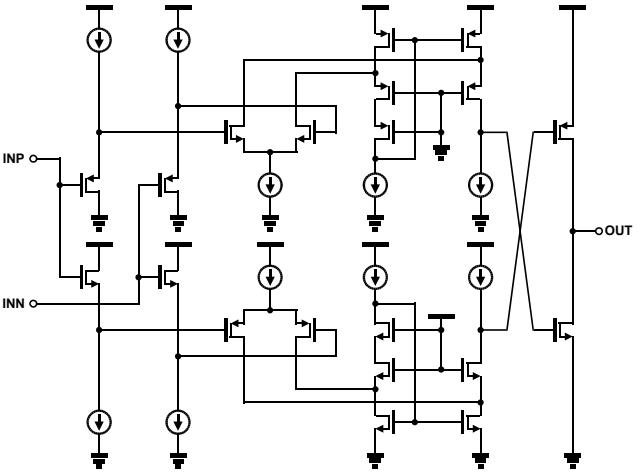

Figure 5. Circuit diagram of the proposed low power wideband op amp.

TABLE I. Simulated Peformance summary of the Op Amp

DC voltage gain	60 dB
3-dB bandwidth	12 MHz
Unity-gain bandwidth	937 MHz
Phase margin	59 °
Slew rate	± 880 V/μs
Power consumption	1.5 mW @ 1.0 V
Core area	0.0064 mm^2
Technology	0.18-μm standard CMOS

IV. Measurement Results

The proposed receiver AFE was fabricated with 0.18-μm standard CMOS technology, where the threshold voltage for NMOS and PMOS at saturation region are 0.58V/-0.58V, respectively. Fig. 6 shows the chip microphotograph. Its active area is about 0.04-mm^2. The test chip was mounted on a FR-4 PC board by using chip-on-board. The prototype of the wrist-type test board powered by a coin battery of 3.0-V is shown in Fig. 7. The supply voltage of the AFE is generated by using an off-chip linear regulator on the board.

The board size is about 3.5cm by 4.5cm. All measurements were conducted between the wrist and the fingertip that corresponds to the distance of about 25cm. The electrode on the backside of the board is touched to the wrist. When the fingertip touches the electrode of a transmitter board, the binary data is transmitted through the body to the wrist-type test board. Fig. 8 shows the measured timing diagram of the input and output signals of the AFE exploiting WST technique for 10-Mb/s 2^7-1 PRBS transmitted data. The received input signal is measured to be about 50-mV amplitude. The preamplifier amplifies the received input signal with the voltage gain of about 30-dB before triggering at the following schmitt trigger. The recovered output exhibits almost 50% duty cycle due to the symmetric operation. The measured 3-dB frequency spectrum of the AFE is in the range of 1-MHz to 200-MHz.

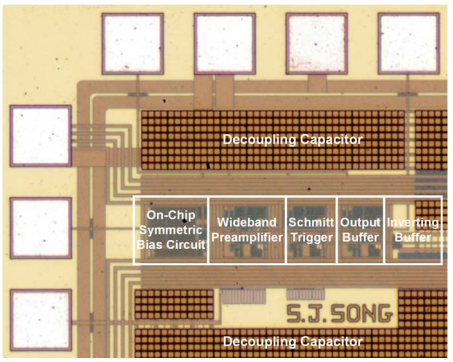

Figure 6. Chip microphotograph.

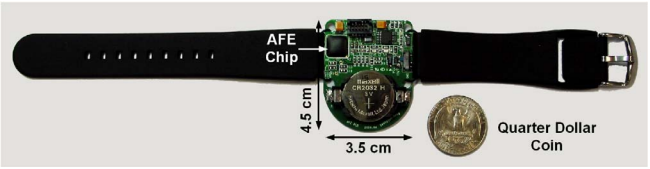

Figure 7. Prototype of wrist-type test board.

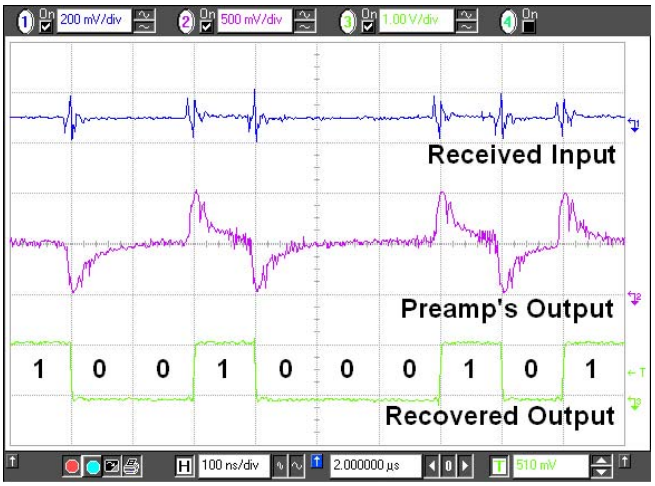

Figure 8. Measured timing diagram of the AFE for 10-Mb/s 2^7-1 PRBS.

Table II summarizes the performance of the AFE. The AFE achieves the reception bit energy of 0.48-nJ/bit, which is 20 times more efficient than the UWB receiver in [4]. Therefore, the proposed AFE provides energy-efficient communications around the human body.

TABLE II. PEFORMANCE SUMMARY OF THE AFE

Data rate	10 Mb/s
Input impedance	50 Ω
3-dB bandwidth	1 ~ 200 MHz
Voltage gain	30 dB
Input sensitivity	-27 dBm
Power consumption	4.8 mW
Supply voltage	1.0 V
Core area	0.04 mm^2
Technology	0.18-µm standard CMOS

V. CONCLUSION

In this paper, an energy-efficient wideband signaling receiver AFE exploiting wideband symmetric triggering technique is presented for the human body as a data transmission medium. The AFE delivers 10-Mb/s data rate with -27-dBm sensitivity and 200-MHz bandwidth. To minimize its power consumption along with wide bandwidth operation, the low-voltage fully complementary folded cascode op amp topology is adopted. The op amp shows 60-dB DC gain and 684-MHz GBW and consumes 1.5mA. The 0.18-µm CMOS receiver AFE dissipates less than 5-mW at a 1-V supply. The achieved performance of the AFE is used for the HBC and show 10-Mb/s data transmission successfully.

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